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Search Results - Record(s) 1 through 9 of 9 returned.

☐ 1. Document ID: US 6792582 B1

Using default format because multiple data bases are involved.

L47: Entry 1 of 9 File: USPT Sep 14, 2004

US-PAT-NO: 6792582
DOCUMENT-IDENTIFIER: US 6792582 B1

TITLE: Concurrent logical and physical construction of voltage islands for mixed supply voltage designs

DATE-ISSUED: September 14, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Cohn; John M	Essex Junction	VT		
Dean; Alvar A.	Groton	MA		
Hathaway; David J.	Underhill Center	VT		
Lackey; David E.	Jericho	VT		
Lepsic; Thomas M.	Jeffersonville	VT		
Lichtensteiger; Susan K.	Essex Junction	VT		
Tetreault; Scott A.	Franklin	VT		
Ventrone; Sebastian T.	South Burlington	VT		

US-CL-CURRENT: 716/7; 326/38, 716/2, 716/4, 716/9

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 2. Document ID: US 6763506 B1

L47: Entry 2 of 9 File: USPT Jul 13, 2004

US-PAT-NO: 6763506
DOCUMENT-IDENTIFIER: US 6763506 B1

TITLE: Method of optimizing the design of electronic systems having multiple timing constraints

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 3. Document ID: US 6272668 B1

L47: Entry 3 of 9 File: USPT Aug 7, 2001

US-PAT-NO: 6272668
DOCUMENT-IDENTIFIER: US 6272668 B1

TITLE: Method for cell swapping to improve pre-layout to post-layout timing

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 4. Document ID: US 6209122 B1

L47: Entry 4 of 9 File: USPT Mar 27, 2001

US-PAT-NO: 6209122
DOCUMENT-IDENTIFIER: US 6209122 B1

TITLE: Minimization of circuit delay and power through transistor sizing

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 5. Document ID: US 5880967 A

L47: Entry 5 of 9 File: USPT Mar 9, 1999

US-PAT-NO: 5880967
DOCUMENT-IDENTIFIER: US 5880967 A

TITLE: Minimization of circuit delay and power through transistor sizing

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 6. Document ID: US 5461576 A

L47: Entry 6 of 9 File: USPT Oct 24, 1995

US-PAT-NO: 5461576
DOCUMENT-IDENTIFIER: US 5461576 A

TITLE: Electronic design automation tool for the design of a semiconductor integrated circuit chip

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 7. Document ID: US 5218551 A

L47: Entry 7 of 9 File: USPT Jun 8, 1993

US-PAT-NO: 5218551
DOCUMENT-IDENTIFIER: US 5218551 A
** See image for Certificate of Correction **

TITLE: Timing driven placement

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 8. Document ID: US 5003487 A

L47: Entry 8 of 9 File: USPT Mar 26, 1991

US-PAT-NO: 5003487
DOCUMENT-IDENTIFIER: US 5003487 A

TITLE: Method and apparatus for performing timing correction transformations on a technology-independent logic model during logic synthesis

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

☐ 9. Document ID: US 4698760 A

L47: Entry 9 of 9 File: USPT Oct 6, 1987

US-PAT-NO: 4698760
DOCUMENT-IDENTIFIER: US 4698760 A

TITLE: Method of optimizing signal timing delays and power consumption in LSI circuits

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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